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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
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ROBERTSON, D.	2167	30

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DATE MAILED: 02/27/01

This is a communication from the examiner in charge of your application.
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OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 01/08/01 & 01/30/01

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 12-19, 26-29 & 31-37 is/are pending in the application.
Of the above, claim(s) 12-19 & 26-29 is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☒ Claim(s) 31-37 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.
☐ received in Application No. (Series Code/Serial Number) _____.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
☐ Interview Summary, PTO-413
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

--SEE OFFICE ACTION ON THE FOLLOWING PAGES--

This Office action is in response to the filing of a CPA on January 30, 2001.

In this application, even though the claims arguably could be construed as being in "means plus function" form under 35 U.S.C. 112, ¶ 6 (e.g., "a first state machine to..."), they have not been considered to invoke 35 U.S.C. 112, ¶ 6 (see the Supplemental Examination Guidelines for Determining the Applicability of 35 U.S.C. 112, ¶ 6 dated June 16, 2000).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of applicant's admitted prior art or, Terada *et al.* (5,561,628).

Applicant's admitted prior art teaches that it was known in the prior art to suspend flash memory erase cycles because of the length of time required for the erase cycle (see specification, lines 1-2). Further, applicants admit that status registers typically store data indicative of the current device status, including whether or not an erase operation has been suspended (see figure 1, memory location 104, "ESS"). Applicants also admit that the stored status was output when the device was polled or in response to a read status register command (see specification, page 2,

lines 3-7). The memory array in applicant's described prior art is understood. Applicants do not admit that suspension of a programming operation was taught in the prior art. However, while a programming operation does not take as long as an erase operation, it still takes a significant amount of time relative to data read operation (7-8 microseconds as opposed to 85 nanoseconds, see specification, page 1, lines 22-25). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified applicant's admitted prior art to include the ability to suspend programming operations to improve the overall performance of a flash memory device. Such a modification, would clearly involve the modification of the status register to include at least one bit to indicate the suspension status of a programming operation (e.g., a "PSS" bit similar to the admitted "ESS" bit). Applicants do not discuss the existence in the prior art of a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state machines to execute the command received by the first state machine. However, such implementation is typical, i.e., a command decoder (i.e., a first state machine) is required to determine what type of command has been received, whether it is a valid command, whether it can be executed, etc. If the command can indeed be executed, the command is typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly applicant's admitted prior art receives a command (i.e., "when polled" or "in response to a read status register command", see specification, page 2, lines 4-7) and then executes the command (i.e., "the status signal may be sent...via a designated output pin" or "via the data input/output

('I/O') pins", *ibid*). It is inherent that applicant's admitted prior art includes the claimed first and second state machines. Further, the admitted prior art programming operation inherently would have included a "byte write" (or "byte program") instruction (claim 32) since that was the typical manner of writing to flash memories. Obviously that would be the programming operation to suspend (claim 33). It is also obvious that the status register read operation of applicant's admitted prior art would output the contents of the status register as modified above, including the write suspend status (claim 34). A device as described above would inherently include the ability to input requests and output data (claim 35). Applicant's admitted prior art includes the ability to be polled or receive a read status register command, it would have been obvious to retain such abilities (claims 36 and 37).

The Terada *et al.* reference teaches, *inter alia*, flash EEPROMs (see figure 3, flash memories 40a through 40d) with the ability to suspend erase cycles, and a status register that outputs an erase suspend status signal when the status register is read (see column 10, lines 47-59 and tables 1 and 2. The memory array *per se* is understood. Terada does not teach the suspension of a programming operation. However, while a programming operation does not take as long as an erase operation, it still takes a significant amount of time relative to data read operation. In a particular 8M-bit IC card it "takes one second or less to read all the addresses on one flash memory, 9.6 seconds to write in all the addresses in one flash memory, and 25.6 seconds to erase from all the addresses of one flash memory", see column 5, lines 5-11). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to

which said subject matter pertains to have modified the memories taught by Terada to include the ability to suspend programming operations to improve the overall performance of a flash memory device. Such a modification, would clearly involve the modification of the status register to include at least one bit to indicate the suspension status of a programming operation (e.g., a "PSS" bit similar to bit 6, "ESS", see tables 1 and 2). Terada does not discuss a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state machines to execute the command received by the first state machine. However, such implementation is typical, i.e., a command decoder (i.e., a first state machine) is required to determine what type of command has been received, whether it is a valid command, whether it can be executed, etc. If the command can indeed be executed, the command is typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly Terada's flash memories receive a command (i.e., "can be read", see column 10, lines 53-55) and then executes the command (i.e., "via a data bus for transmitting signals D0 to D15", *ibid*). It is inherent that Terada includes the claimed first and second state machines. Further, each of the Terada flash memories operates in a "byte write" (or "byte program") mode (see table 2, SR.4, claim 32). Obviously that would be the programming operation to suspend (claim 33). It is also obvious that Terada's status register read operation would output the contents of the status register as modified above, including the write suspend status (claim 34). A device as described above would inherently include the ability to input requests and output data (claim 35). Terada's flash memories clearly can be polled or otherwise (claims 36 and 37).

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leak *et al.* (5,937,424) in view of Terada *et al.* (5,561,628). The Leak *et al.* reference teaches a memory device which includes a memory array (understood), a register to store status information (see figure 7B, status register 142), a control circuit including a command decoder (first state machine) and a second state machine (see figure 7B, any of elements 190, 192, 194, 195, 196 and 198. The reference further teaches that it is advantageous to be able to suspend both erase and write operations. The reference does not teach the particulars of the status register. The Terada reference has been discussed above. It teaches a status register that includes an "ESS" bit to indicate the erase suspend operation status. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modeled Leak the status register after the Terada status register to include an "ESS" bit to indicate that an erase operation has been suspended, and to further have modified the Terada status register to include a "WSS" bit to indicate that a write operation has been suspended. By the comparisons to the prior art, it appears that Leak operates in byte write mode and that the byte write operation is suspended (claims 32 and 33). In keeping with the modification above, note that Terada teaches that if ESS = 1, an erase operation is suspended, if ESS = 0, then no erase is suspended. The above modification would, by analogy, indicate that if WSS = 1, then a write operation is suspended and if WSS = 0, then no write operation is suspended (claim 32). The Leak command decoder has an input and clearly receives a status request signal to activate

read status circuitry 198 (see figures 7A and 7B). The status register apparently outputs the status data on line RY/BY# (see figure 7B), presumably only upon request (claims 36 and 37).

Applicant's arguments filed January 8, 2001 have been fully considered. The amendment overcomes the 35 U.S.C. 112 rejections.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-6306, (for formal communications intended for entry)

Or:

(703) 308-6306 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the technology center receptionist whose telephone number is **(703) 305-3900**.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Robertson whose telephone number is (703) 305-3825.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached at 308-4908. **The fax number for this Technology Center is (703) 308-6306.**

Communications which are not application specific may also be posted on e-mail at *David.Robertson@USPTO.gov*.

DAVID L. ROBERTSON
PRIMARY EXAMINER
ART UNIT 2187

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February 23, 2001